

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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Title of Invention

STRUCTURE AND METHOD OF FORMING A BIPOLAR
TRANSISTOR HAVING A VOID BETWEEN EMITTER AND
EXTRINSIC BASE

Application Number :

Confirmation Number:

First Named Applicant: Rama Divakaruni

Attorney Docket Number: FIS920030414US1

Art Unit:

Examiner:

Search string: (5128271 or 5494836 or 5506427 or 5962880 or 6346453 or 20030057458 or
20030109109).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
1	1	5128271	1992-07-07	Bronner, et al.			
2	2	5494836	1996-02-27	Imai			
3	3	5506427	1996-04-09	Imai			
4	4	5962880	1999-10-05	Oda, et al.			
5	5	6346453	2002-02-12	Kovacic, et al.			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
1	1	20030057458	2003-03-27	Freeman, et al.			
2	2	20030109109	2003-06-12	Freeman, et al.			

Signature

Examiner Name	Date
John Bah	8/24/04



Not Yet Assigned

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

M.W. Xu et al. "Ultra Low Power SiGe:C HBT for 0.18 μ m RF-FiCMOS, " Proceedings of the IEEE International Electron Devices Meeting, 2003.

***EXAMINER:** Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.